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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,438	07/12/2004	Yung-Ming CHIU	REAP0068USA	4437
27765 7.	590 06/12/2006		EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			STERRETT, JEFFREY L	
			ART UNIT	PAPER NUMBER
•			2838	·

DATE MAILED: 06/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)			
	10/710,438	CHIU, YUNG-MING			
Office Action Summary	Examiner	Art Unit			
	Jeffrey L. Sterrett	2838			
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address			
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	N. nely filed the mailing date of this communication.			
Status					
1) Responsive to communication(s) filed on 25 Ag	oril 2006				
	action is non-final.				
, _ ,	ince this application is in condition for allowance except for formal matters, prosecution as to the merits is				
closed in accordance with the practice under E					
Disposition of Claims					
<u> </u>		•			
4) Claim(s) 1-21 is/are pending in the application.					
4a) Of the above claim(s) is/are withdrawn from consideration.					
5) Claim(s) is/are allowed.					
6)⊠ Claim(s) <u>1-21</u> is/are rejected. 7)□ Claim(s) is/are objected to.					
7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or	e election requirément				
	election requirement.				
Application Papers		•			
9) The specification is objected to by the Examiner.					
and 10) The drawing(s) filed on is/are: a) □ accepted or b) □ objected to by the Examiner.					
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
, Replacement drawing sheet(s) including the correcti					
11) The oath or declaration is objected to by the Ex	aminer. Note the attached Office	Action or form PTO-152.			
Priority under 35 U.S.C. § 119					
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of:					
1. Certified copies of the priority documents have been received.					
2. Certified copies of the priority documents have been received in Application No					
3. Copies of the certified copies of the priority documents have been received in this National Stage					
application from the International Bureau	, ,,				
* See the attached detailed Office action for a list of	of the certified copies not receive	d'			
Attachment(s)	·				
1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)					
Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date Notice of Informal Patent Application (PTO-152)					
Paper No(s)/Mail Date	6)	-			

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1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-3, 5-7, 11-13, and 15-17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Calafato et al (US 6,133,718).

Calafato et al discloses a temperature compensated reference generator (Figure 7) comprising a plurality of signal generators (10 and 11) producing a plurality of signals corresponding to a plurality of temperature dependent characteristics, a combining module (12) combining the plurality of signals into a combined signal (Iref) as recited by claims 1-3, 5-7, 11-13, and 15-17 except for utilizing a signal to voltage converter generating a reference voltage from the combined signal. Official notice is taken that signal to voltage converters were old and known expedients in the art at the time of the invention for generating a voltage corresponding a provided signal. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the reference generator of Calafato et al by utilizing a signal to voltage converter to generate a reference voltage from the reference current since current to voltage conversion is nothing more than basic electrical engineering well within the knowledge and experience of said skilled artisan.

3. Claims 4, 14, and 21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Toumazou et al (1/25/06 IDS citation 1).

Toumazou et al discloses a second order temperature compensated reference voltage generator (Figure 5.16) comprising a plurality of signal generators (Vbe1 and

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Vbe2) producing a plurality of signals corresponding to a plurality of temperature dependent characteristics, a combining module (Combiner) combining the plurality of signals into a combined signal, and a signal to voltage converter (Transadmittance) coupled to the combining module for generating a compensated reference voltage (Vout) as recited by claims 4, 14, and 21 except for utilizing at least 3 signal generators. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the reference generator of Tournazou et al by utilizing at least 3 signal generators since it has been held that where the general conditions of the claim are disclosed in the cited and applied prior art, discovering the optimum or workable value of a result effective variable involves only routine skill in the art (In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980)).

4. Claims 8, 9, 18, and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Calafato et al (US 6,133,718).

Calafato et al discloses a reference generator (Figure 7) as explained above and as recited by claims 8, 9, 18, and 19 except for utilizing specific circuitry as each signal generator. Official notice is taken that the specifically recited signal generator circuitry was an old and known expedient in the art at the time of the invention. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the reference generator of Calafato et al by utilizing any old and known signal generator circuitry, such as that specifically recite by applicant, as the signal generators (10 and 11) since said artisan would be expected to utilize which ever old and known signal generator circuitry best suited the situation at hand.

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5. Claims 10 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Calafato et al (US 6,133,718).

Calafato et al discloses a reference generator (Figure 7) as explained above and as recited by claims 10 and 20 except for utilizing a resistor as the signal to voltage converter. Official notice is taken that utilizing a resistor as a signal to voltage converter to generate a reference voltage from a reference current was an old and known expedient in the art at the time of the invention. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the reference generator of Calafato et al by utilizing a resistor as the signal to voltage converter since this is nothing more than basic electrical engineering utilizing the relationship of current through a resistor to the voltage across the resistor, V=IR.

6. Applicant's arguments filed April 25, 2006 have been fully considered but they are not persuasive.

In response to the remarks regarding utilizing a resistor as the signal to voltage generator, whether Calafato et al teaches away from utilizing a resistor as the signal to voltage generator within each current generator (10 or 11) is immaterial. First, Calafato et al discusses the merits of utilizing a resistor within each current generator (10 or 11) NOT as a signal to voltage generator to convert the reference current Iref to a reference voltage. Second, even if Calafato et al is considered to teach away from utilizing a resistor as the signal to voltage generator, it is from the standpoint that doing such was an old and known expedient in the art at the time of their invention that had undesirable side effects (i.e. applicant is taking a step backwards in the art NOT a patentable step forward in the art). Third, it is noted that the original rejection stated that in general

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signal to voltage converters were old and known expedients in the art at the time of the invention for generating a voltage corresponding a provided signal and stated that utilizing a resistor was a basic specific example of such a signal to voltage generator (the rejection is now laid out so that where the claims are general the rejection is general and where the claims are more specific the rejection is more specific). Thus Calafato et al discloses the general level of the prior art before their invention, their assessment of that prior art, and their improvement over that prior art, all of which making the invention set forth by the pending claims unpatentable. It is also noted that any critique by applicant concerning the desirability or nondesirability of utilizing a resistor as a signal to voltage converter is equally valid against applicant's utilization of resistor 330 to generate reference voltage Vref.

In response to the remarks regarding the specific circuitry of each signal generator, although each signal generator may comprise the same basic elements there is nothing that dictates that each signal generator has to have the same temperature gradient. Claims 8, 9, 18, and 19 only require that each signal generator comprise a first and second current sources providing substantially equal currents in response to a control signal, a resistor coupled to the first current source, a transistor with its emitter coupled to the second current source and its base and collector coupled to a supply node, and a control signal generator (operational amplifier in claims 9 and 19) generating the control signal so that the voltage of the resistor is substantially equal to the emitter voltage of the transistor. This recitation allows for different types of current sources to be used in each signal generator as long as each signal generator has any

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two current sources, allows for different types of resistors to be used in each signal generator as long any resistor is used in each signal generator, allows for different types of transistors to be used in each signal generator as long any transistor is used in each signal generator, and allows the control signal generator/operational amplifier to be configure in any way desired as long as each current source has a control signal generator/operational amplifier. Thus it is well within the skill and experience of said skilled artisan to fulfill both the design requirements of Calafato et al (notably that the temperature gradients of the signal generators differ) and the general circuitry design specified by applicant and considered as old and known in the art at the time of the invention.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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than SIX MONTHS from the date of this final action.

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the advisory action. In no event, however, will the statutory period for reply expire later

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8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey L. Sterrett whose telephone number is (571) 272-2085. The examiner can normally be reached on Monday-Thursday & 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl D. Easthom can be reached on (571) 272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeffrey L. Sterrett Primary Examiner Art Unit 2838

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